

FIG. 1 is a block diagram of a system 100 for dynamic code generation. The system 100 includes a transmission source 10, a receiver 20, a data sampling controller 30, a dynamic database controller 40, and a dynamic code database 50. The receiver 20, data sampling controller 30, dynamic database controller 40, and dynamic code database 50 are connected to a common bus 60. The transmission source 10 is connected to the receiver 20 via a bidirectional communication link 70.

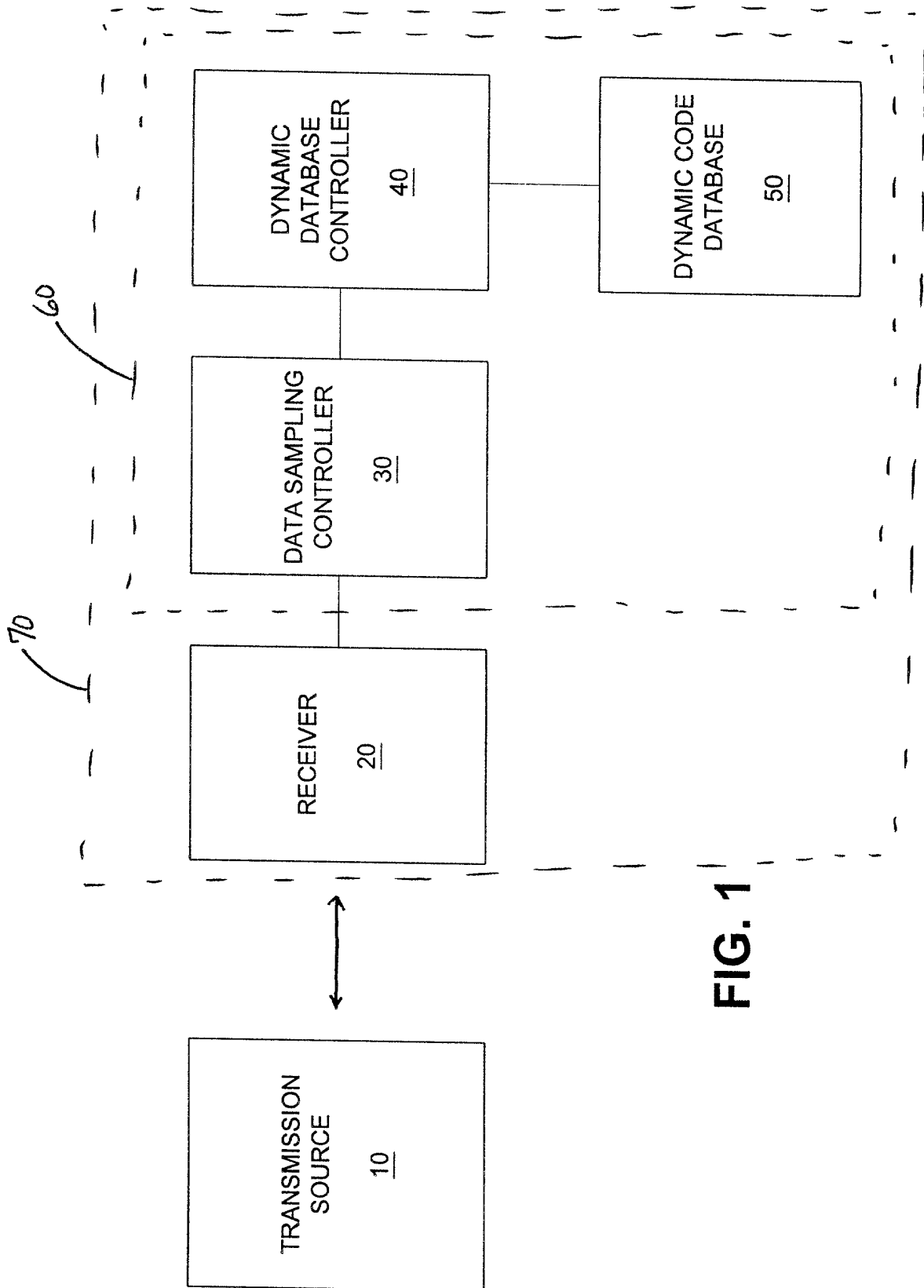


FIG. 1

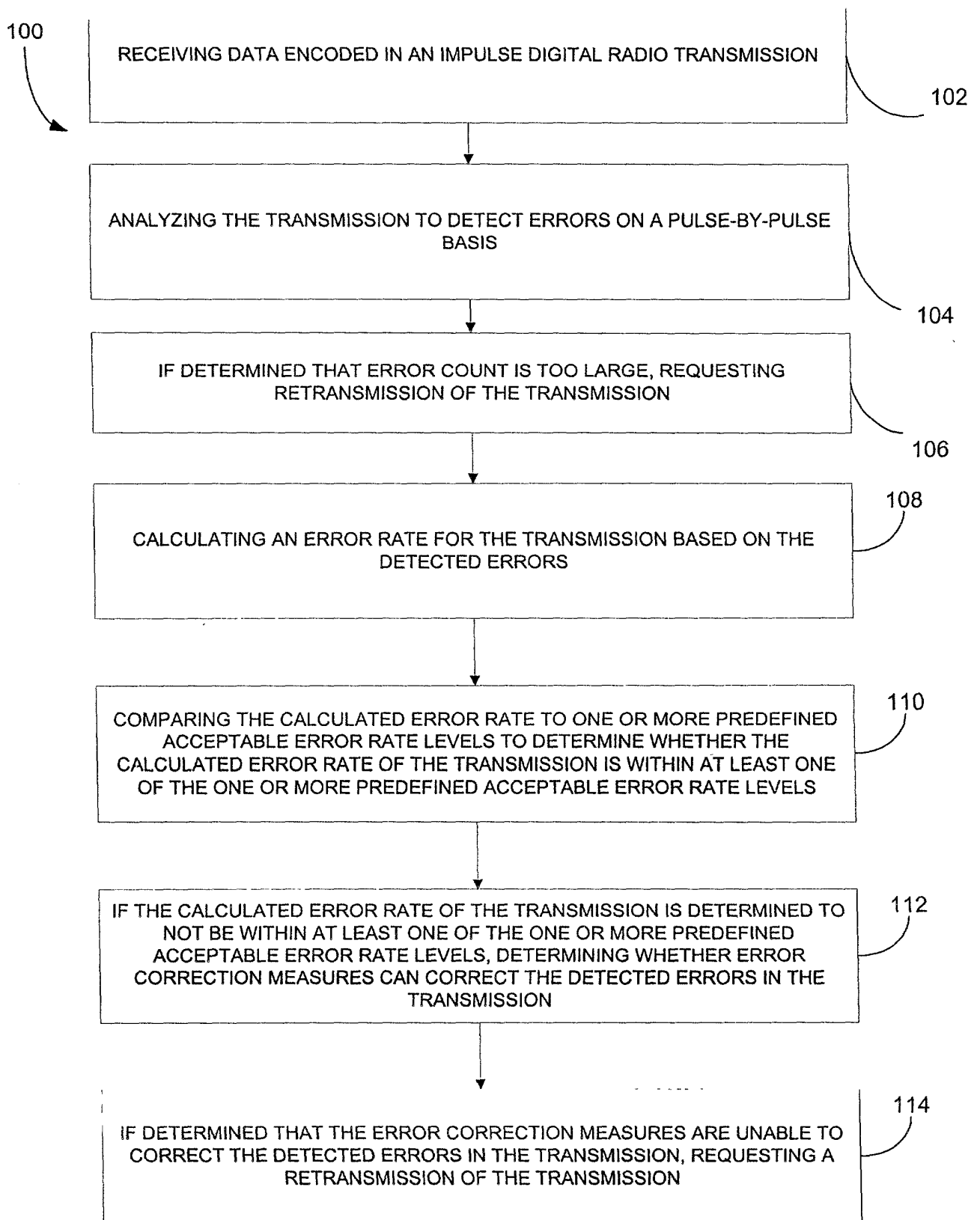


FIG. 2

FIG. 3 is a cross-sectional view of a semiconductor device 200, taken along line A-A of FIG. 1. The device 200 includes a substrate 202, a gate stack 204, and a channel layer 206. The gate stack 204 includes a gate dielectric layer 208 and a gate electrode layer 210. The channel layer 206 is disposed on the substrate 202 and under the gate stack 204. A source region 212 is formed in the substrate 202 on one side of the channel layer 206, and a drain region 214 is formed in the substrate 202 on the other side of the channel layer 206. A source contact 216 is formed on the source region 212, and a drain contact 218 is formed on the drain region 214. A gate contact 220 is formed on the gate electrode layer 210. A gate spacer 222 is formed on the side of the gate electrode layer 210. A gate cap 224 is formed on the top of the gate electrode layer 210.

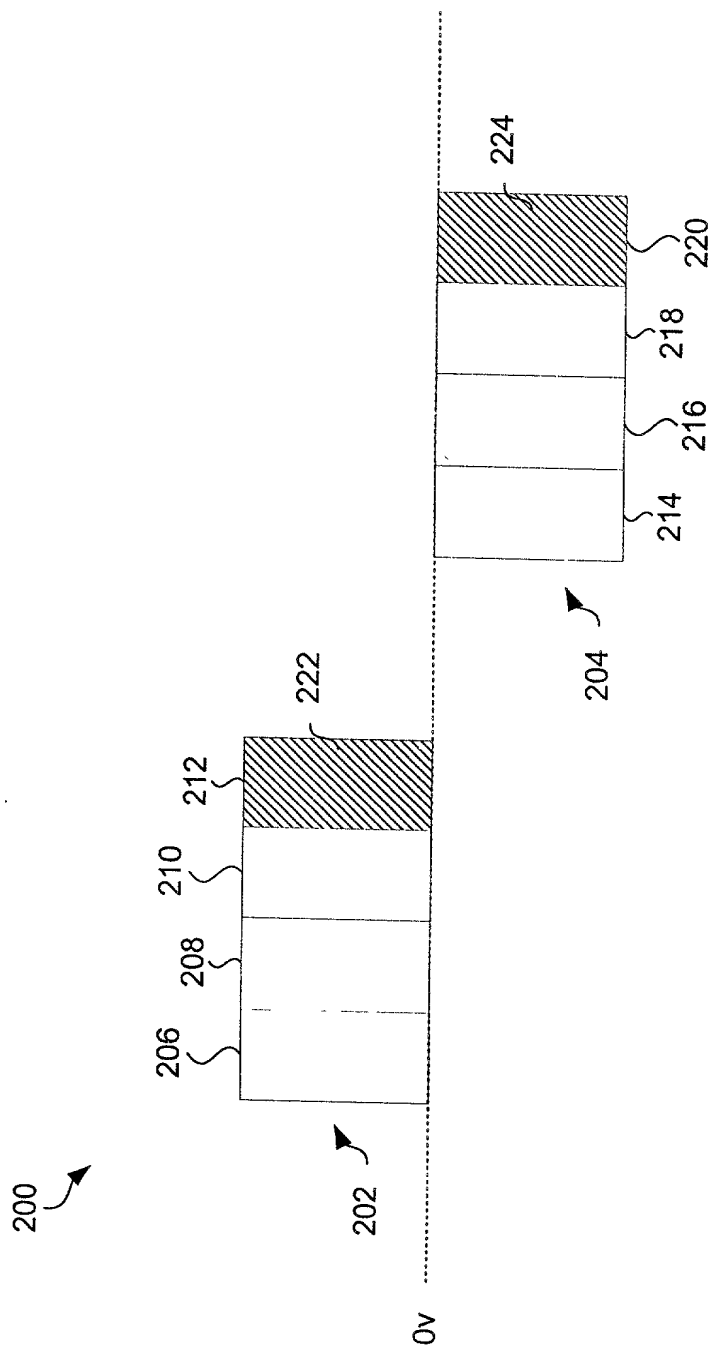


FIG. 3

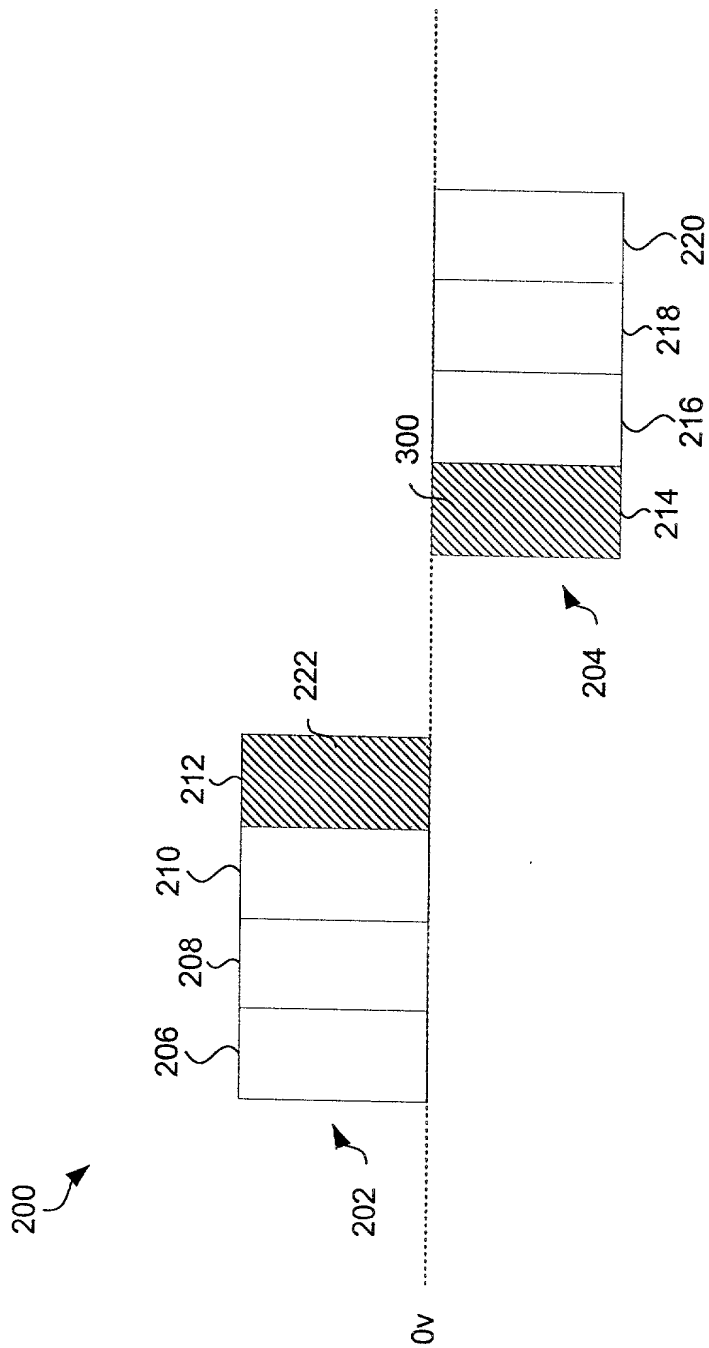


FIG. 4

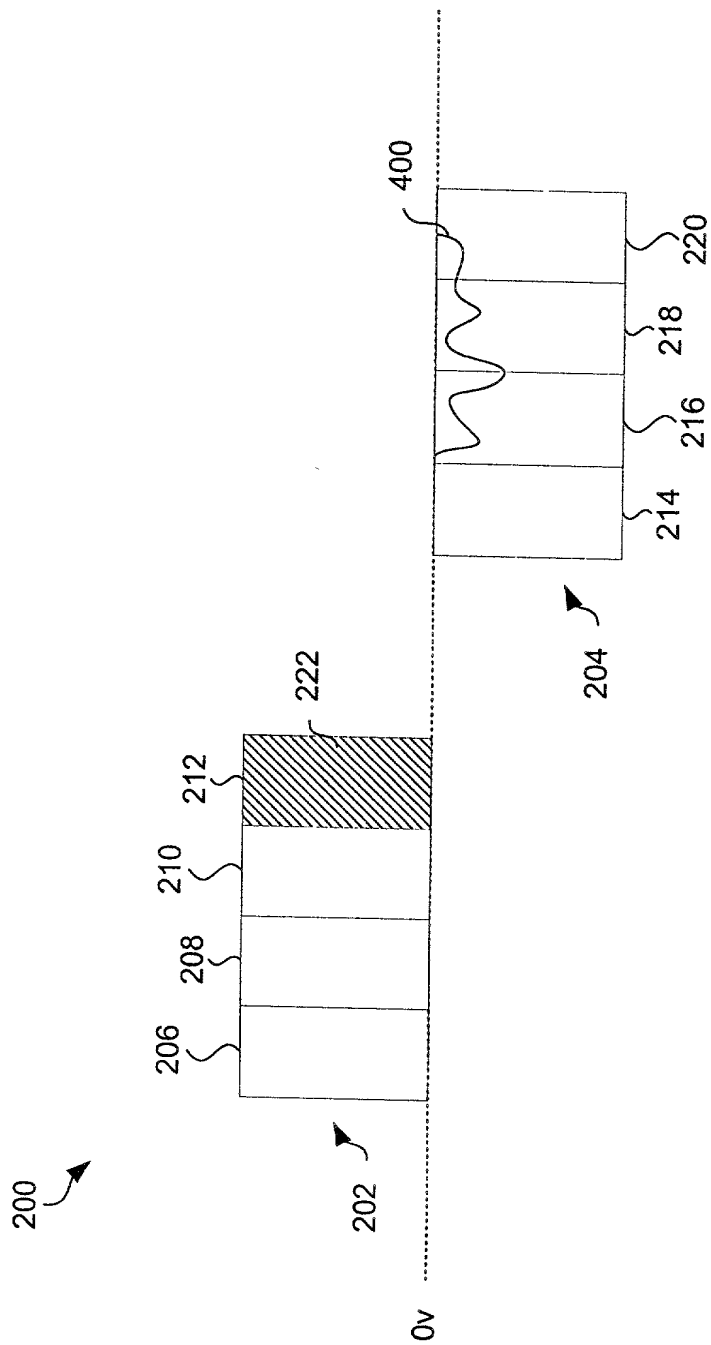


FIG. 5

FIG. 6 is a cross-sectional view of a semiconductor device 200, showing a substrate 202, a gate stack 204, and a source/drain region 206. The gate stack 204 includes a gate dielectric layer 208 and a gate electrode layer 210. The source/drain region 206 includes a source/drain dielectric layer 212 and a source/drain electrode layer 214. A channel region 216 is formed in the substrate 202 between the source/drain regions 206. A contact layer 218 is formed on the source/drain electrode layer 214. A passivation layer 220 is formed on the contact layer 218. A solder bump 222 is formed on the passivation layer 220. A dashed line 500 indicates the top surface of the substrate 202.

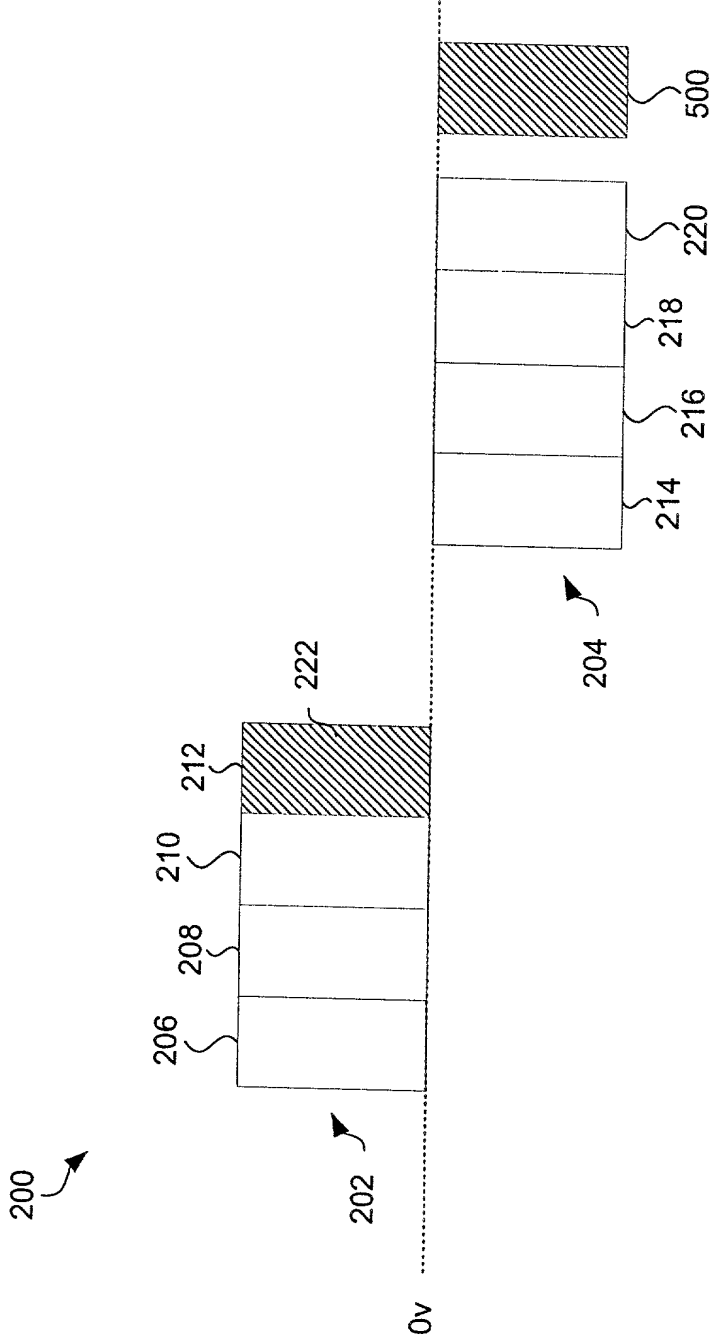


FIG. 6

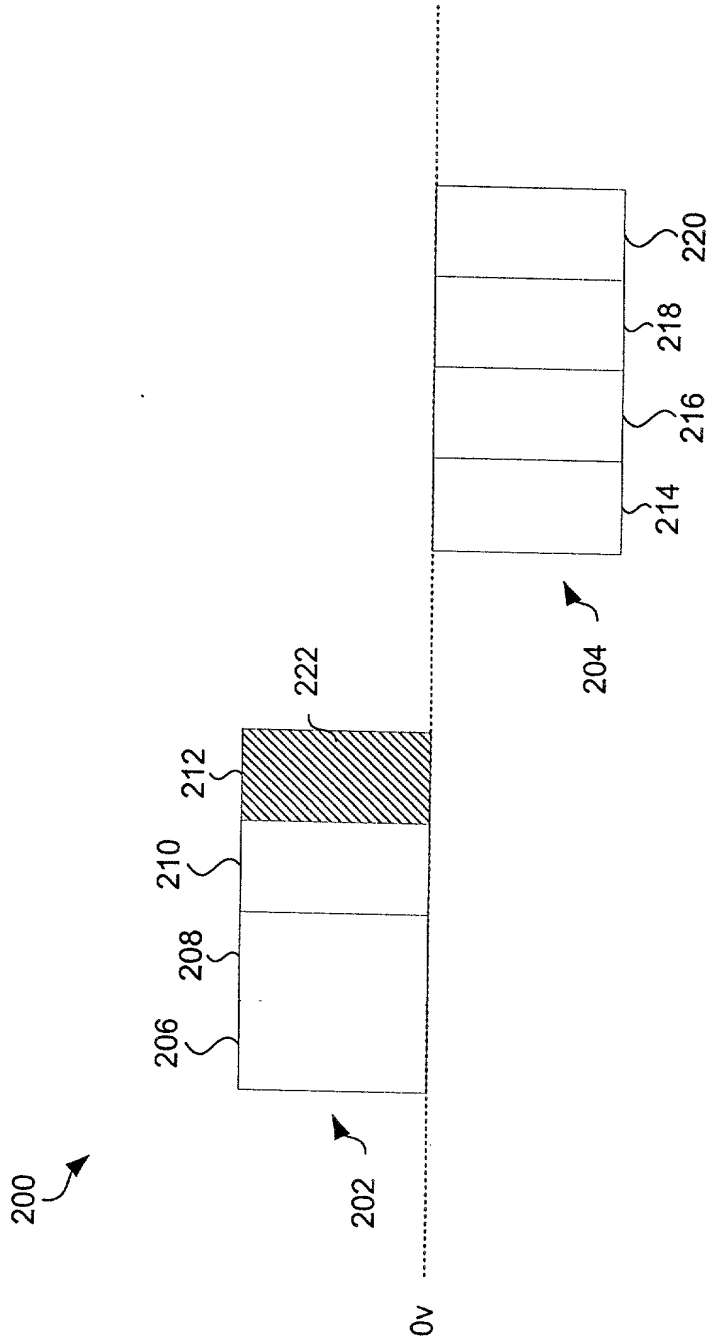


FIG. 7

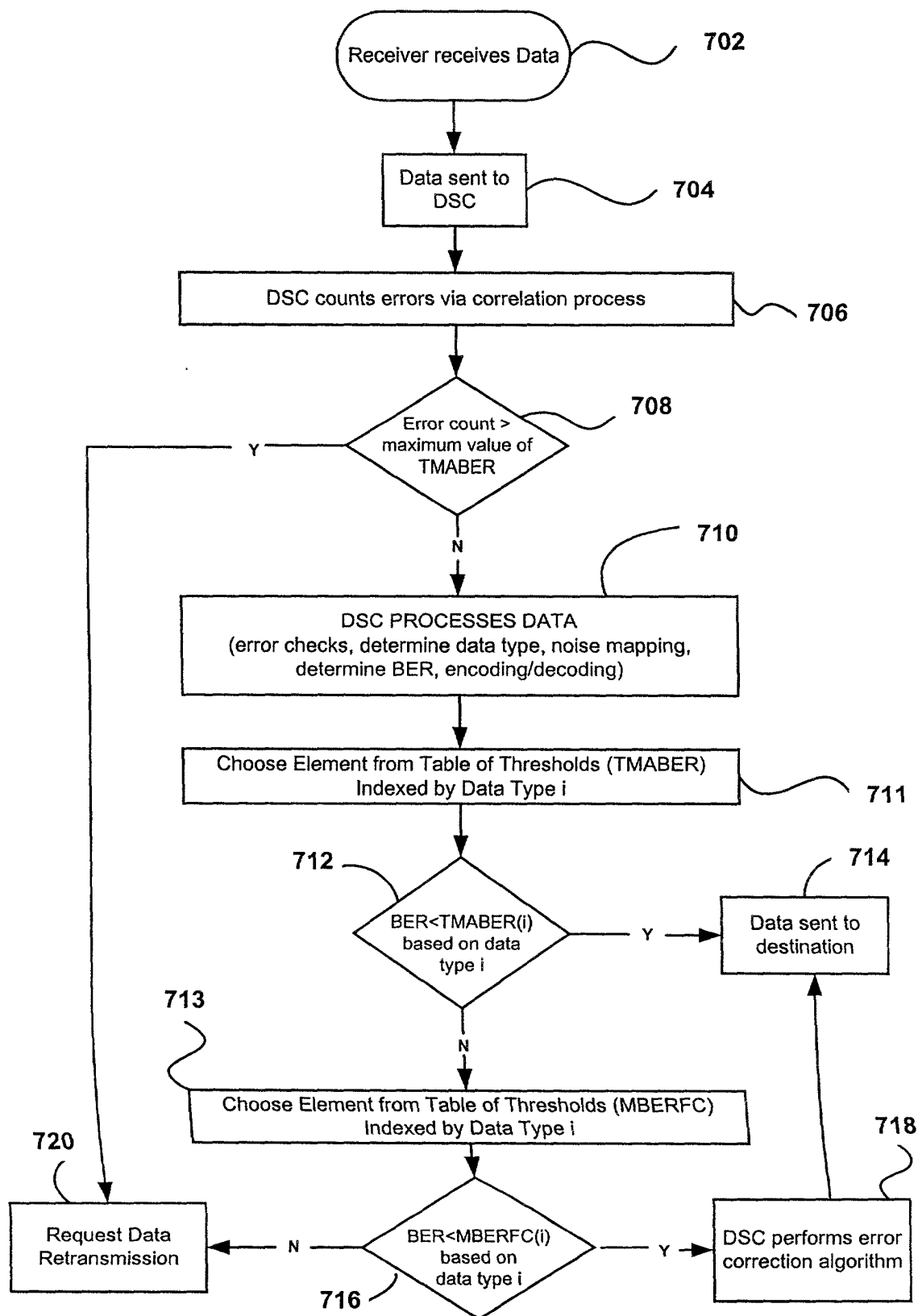


FIG. 8

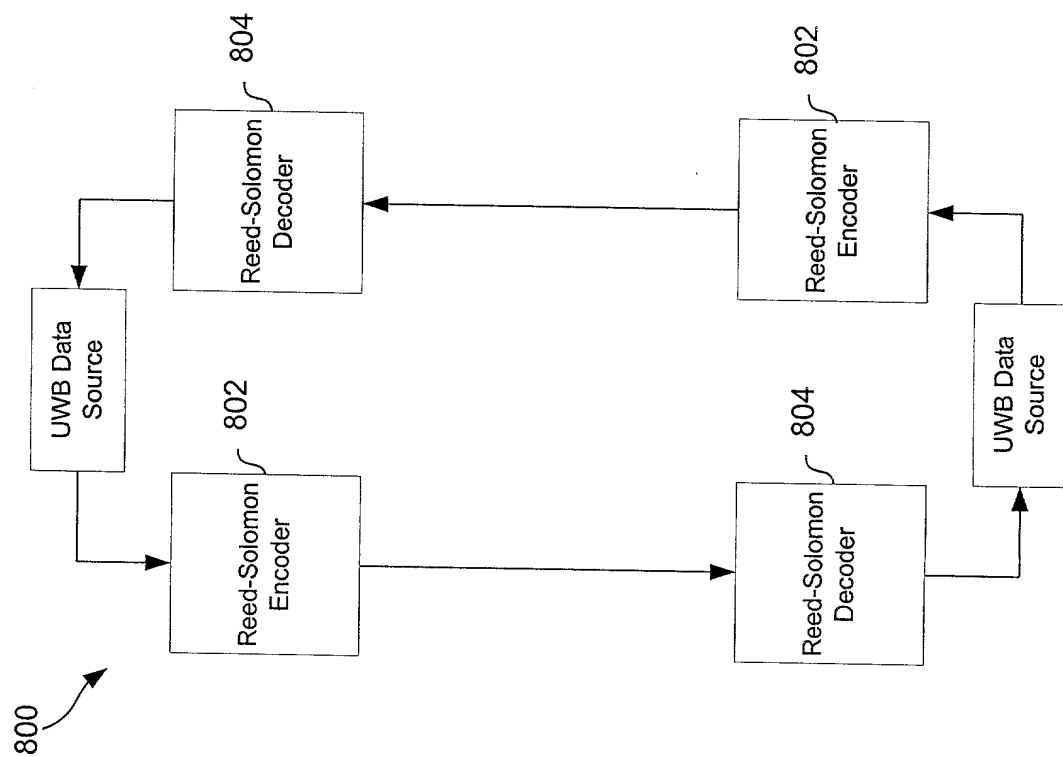


FIG. 9

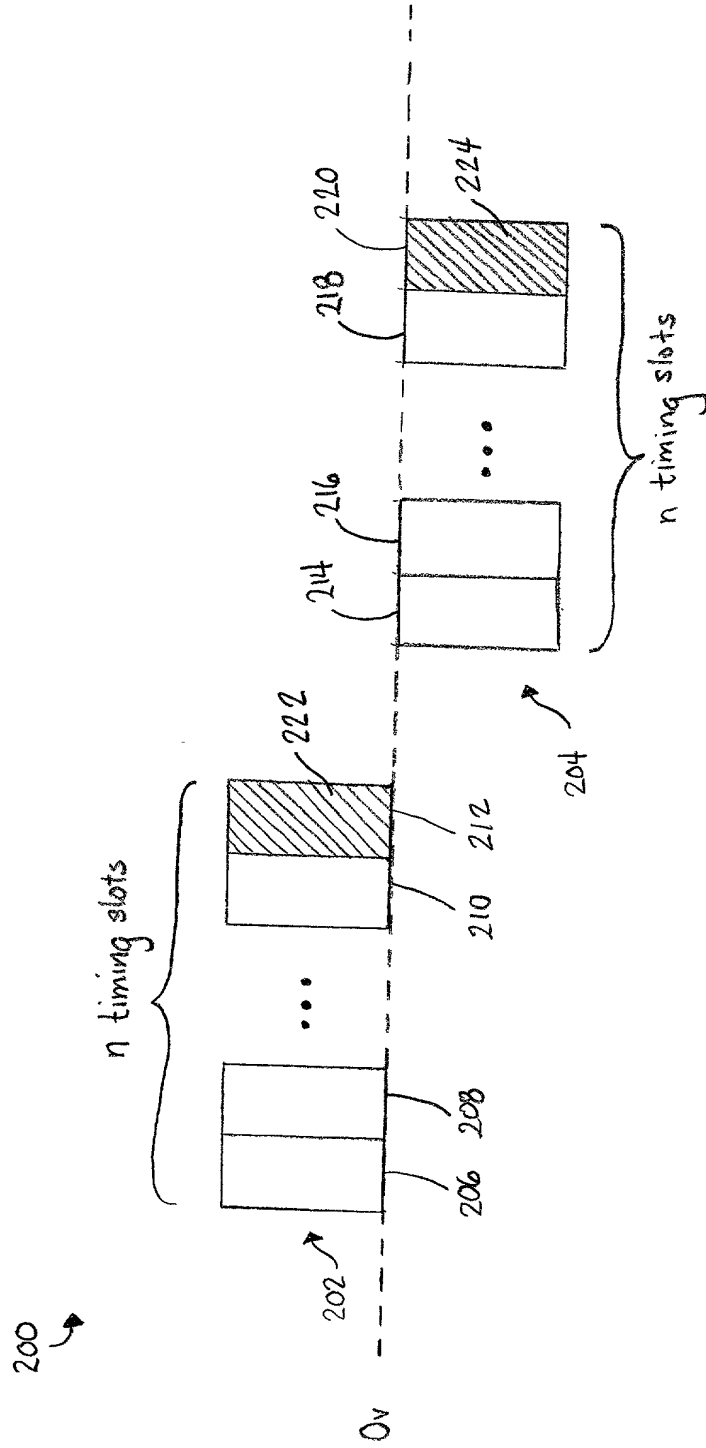


FIG. 10